Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2018) 26: 2347 – 2360

doi:10.3906/elk-1712-353

A low-cost and flexible architecture of digitally controlled DC-DC converter to improve dynamic performance

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Received: 26.12.2017 • **Accepted/Published Online:** 20.05.2018 • **Final Version:** 28.09.2018

Abstract: One type of DC-DC converters is dual transistor forward converter. In this article, a low-cost architecture of a digital controller for dual transistor forward converter is presented. This architecture is designed by using the finite set model predictive control technique. Based on this approach, a low-cost fixed-point arithmetic architecture with minimum functional units is presented to find the optimum switching time at each sampling point. Charge balance control method is utilized to improve the dynamic performance of the transient response. The proposed architecture is implemented and realized by using a field-programmable gate array (FPGA) platform to evaluate the precision of the fixed-point calculation. Several cases for different loading conditions for different word lengths are practically investigated and the proposed digital controller shows a minimum voltage overshoot–undershoot and short settling time under load-changing situations. Compared with other controllers, the presented work provides a better dynamic performance and lower implementation cost.

Key words: Forward converter, digital controller, predictive control, fixed-point computations, low-cost architecture, word length

1. Introduction

In recent years, the control of power switching converters has been widely studied and new algorithms are introduced. There are many applications of forwarding converters in low-voltage and high-current circuits [1–4]. In the analog implementation of controllers, many control algorithms have been introduced to modify dynamic response of converters [5–8]. Transient performance is modified in [5] by using load current feedforward compensation. In [6,7], by employing hysteretic current mode controllers, a quick dynamic performance of the system is presented, where the ordinary feedback compensation network is deleted. Although presented algorithms are capable of achieving the optimum performance in terms of minimum undershoot–overshoot and transient time, generally, due to complex mathematical computations requirements, hardware or embedded system realization of the algorithms is challenging. The benefits of digital control in comparison with analog control are programmability, easiness of intricate arithmetic, and reliability [9].

In [9], a digital controller predicts the optimum transient time for a DC-DC converter by employing the charge balance control (CBC) technique during transient times. In [10] various techniques for design and control of DC-DC converters are presented. In [11] the dynamic response of the power converter is modified by using two segregate control techniques for steady state and transient situations. In [12] a digital controller is

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considered for dual transistor forward converter to improve the dynamic response during a transient state. The optimum switching state is selected using CBC. Here positive and negative load current changes are verified. In [13–15], for DC-DC power converters other digital optimum techniques are investigated, but unfortunately, these techniques have one of the following drawbacks: complex mathematical operations, or slow reaction to load-change conditions.

In this article, the main purpose is to analyze the fixed-point implementation of a digital controller for a DC-DC converter using finite control set model predictive control (FCS-MPC). Accordingly, corresponding computation accuracies are evaluated for different word lengths. The proposed controller has a low-cost architecture with minimum functional units, and is flexible in terms of word length, implementation cost, speed, and output accuracy. There is a trade-off between these parameters, for example, higher word length causes high implementation cost and low processing speed.

As a proof of concept, the controller is implemented on an FPGA platform. The FPGAs are widely used in implementation and prototyping of different control algorithms. The biggest issue in the most of previous approaches, however, is their hardware design approach. Since hardware implementation of the control algorithm is a multidisciplinary field, it is a challenge for power electronic designers to consider and solve both control algorithm issues and hardware design efficiency at the same time. Our approach presents a new direction in this regard.

In previous works, controllers are implemented using based block diagram high-level synthesis tools. These synthesis tools provide an easy design platform using a functional description of the algorithm, but design details are hidden from the designer, which makes it suitable for lab prototyping of the design, but it is not applicable for industrial designs in which the designer needs an optimized implementation suitable for embedded or integrated circuit hardware realization. For instance, accuracy and implementation cost (bit width vs. required hardware) are normally ignored in automated design synthesis. Further, without deep knowledge of hardware design and synthesis, proper trade-offs between different implementation costs such as speed, reliability, precision, and power consumption are not possible.

We are introducing a design method based on a predefined soft architecture in which a hardware data path is synthesized. This approach provides a solution for power electronic engineers by which they can design efficient control hardware with minimum cost. This is different from a microcontroller-based approach, which is limited to the hardware resources available on the microcontroller chip. Also, it is different from other FPGA-based approaches and automatic synthesis tools, which either offer simplified drag and synthesis methods by hiding design complexity or offering a large amount of hardware and FPGA parameters and professional design details.

The controller design in this paper is optimum in terms of required resources (only two adders and two multipliers), which makes it an efficient candidate for an integrated circuit implementation of this controller. To the authors' best knowledge, this is the first article that stated application of model predictive control for a dual transistor forward converter.

In this controller, if any change appears in the output voltage, this technique predicts the behavior of future load voltage for each switching state of the dual-transistor forward converter (DTFC). The cost function compares predicted value for settling time with its reference to minimize the error at each sampling time. Then the optimal switching states with minimum cost function are applied to the semiconductor switches, so by changing the frequency of the gate signals, the controller adjusts the output voltage under the positive and negative load current step changes in the shortest possible time. If the deviation in the output voltage is not

seen, the controller adjusts the output voltage by using linear control. In this state, the frequency of gate signals is constant.

The paper is formed as follows: in Section 2, the operation of the DTFC and CBC are analyzed, and in Section 3, an implemented architecture based on predictive control is presented. In Section 4, results are covered and the conclusions are represented in Section 5.

2. Control of the DTFC with charge balance control (CBC)

In Figure 1, the structure of a DTFC is depicted. It comprises the following elements: Metal oxide semiconductor field effect transistor (MOSFET) switches (S_1, S_2), transformer (T_1), rectifier diode (D_3), a freewheeling diode (D_4), and an output filter (L, C). When transistors S_1 and S_2 are turned off, the transformer magnetizing current flows through the two forward-biased diodes D_1 and D_2 and then backs into the source. The diodes conduct all the magnetizing energy in the primary, along with the energy stored in the leakage inductances, to the input supply. Since diodes D_1 and D_2 clamp the input voltage, no snubber circuit is required. Any overshoot beyond the input voltage needs to be managed with a proper circuit layout to minimize stray inductances. On the secondary winding, the freewheeling diode conducts and transfers the output inductor energy to the load. During the nonpower delivery cycle of the primary, proper transformer reset time is achieved when the ON time is less than its OFF time (duty cycle is less than 50%). In other words, the primary winding itself acts as the reset winding. Having the OFF time longer than the ON time will always reset the transformer.

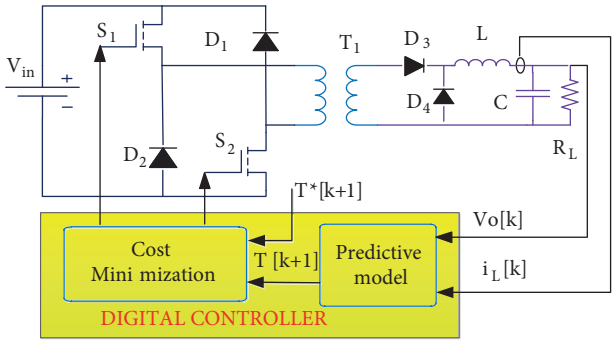

Figure 1. Structure of a DTFC and digital FS-MPC controller.

In the following equation, the concept of CBC over the transient time is represented:

$$v_c(t_b)\, v_c(t_a) = \frac{i_{cavrege}}{C} = 0 \rightarrow \frac{\int_{t_a}^{t_b}(t)dt}{t_b - t_a} = 0 \tag{1}$$

In this equation t_a is the beginning of the transition time, and t_b is the end of the transition time. If we accept Eq. (1), which indicates the DC output voltage turns to the reference voltage after a transition time, and furthermore, if at time t_b the current i_L corresponds to the new load current, the converter would return from a transient time. This idea can be applied to minimize the voltage ripples and predict the optimal settling time. In this study, two cases of positive and negative load current step changes are considered.

2.1. Positive load current step change

In this case, the output voltage and inductor current are shown in Figure 2a. At the start of the transition, the capacitor should be discharged since the inductor current cannot change immediately; the capacitor provides a

section of the load current that causes the reduction in the output voltage from its reference. Once i_L goes up to the new load current at t_3 as shown in Figure 2a, the capacitor begins to recharge and the output voltage rises. During T_3, i_L diminishes from its maximum slew rate. At t_5, when both of i_L and v_o reach their new steady-state values, the DTFC will come around from a positive load step. According to this figure, the whole transition time consists of two sections: discharge section (A_1) and the recharge section (A_2). Therefore, the main purpose of this algorithm is to compute T_1, T_2, and T_3 exactly and minimize them. For this purpose, the discharge section (A_1) and the recharge section (A_2) must be calculated initially. A_1 and A_2 have unusual shapes. The easy technique for calculation of these areas is to approximate them as triangular shapes [12]. Accordingly, an approximation of A_1, A_2 for a positive load step is depicted in Figure 2b. The mathematical bases are represented briefly as follows.

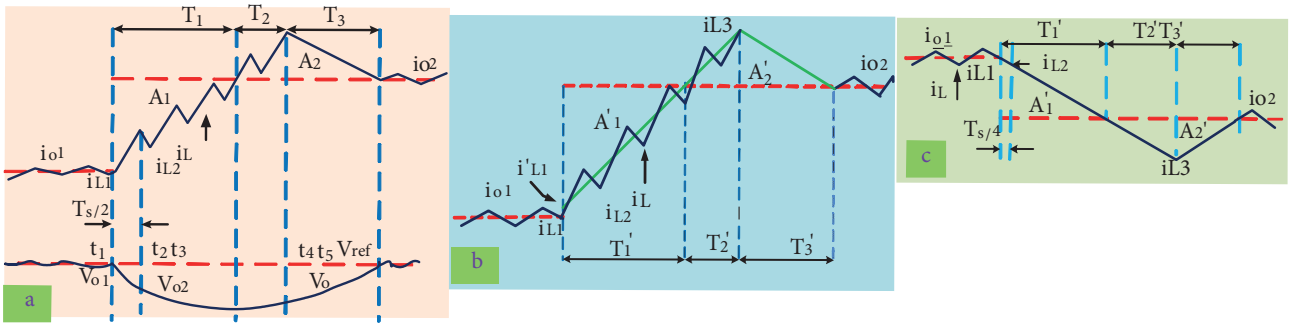

Figure 2. Performance of the DTFC. a) Positive load current step. b) Approximation of A1 and A2 for positive load step. c) Proximate computation of A1, A2 for a negative load step.

By measuring the inductor currents i_{L1}, i_{L2}, and the output voltages v_{o1}, v_{o2} at t_1 and t_2, the new load current i_{o2} can be calculated as:

$$i_{o2}=\frac{1}{2}\left(i_{L1}+i_{L2}\right)-2\frac{C}{T_s}(v_{o2}-v_{o1}). \tag{2}$$

The rising slew rate and falling slew rate of the inductor current are computed as:

$$\frac{di_L}{dt}|_{fall}=-\frac{v_o}{L}=-m_2\frac{di_L}{dt}|_{rise}=\frac{S_1S_2nv_{in}-2v_o}{2L}=m_1,\frac{di_L}{dt}|_{fall}=-\frac{v_o}{L}=-m_2 \tag{3}$$

where v_{in} is the input and v_o is the output voltage, n is the turns ratio of the transform, and S_1, S_2 are switching states which are 0 and 1: 0 when the switch is open and 1 when is closed.

According to these equations:

$$T_1^{'}=\frac{i_{o2}-i_{L1}^{'}}{m_1}A_1^{'}=\frac{1}{2}T_1^{'}(i_{o2}-i_{L1}^{'}), \tag{4}$$

in which $i_{L1}^{'}$ is the refined inductor current in Figure 2b and can be calculated as

$$i_{L1}^{'}=i_{L1}+\frac{S_1S_2nv_{in}}{L}\frac{T_s}{8}. \tag{5}$$

To have a CBC algorithm, $A_1^{'}$ must equal to $A_2^{'}$, and $A_2^{'}$ can be calculated as

$$A_2^{'}=\frac{1}{2}(T_2^{'}+T_3^{'})\left(i_{L3}-i_{o2}\right)i_{L3}=i_{o2}+m_2T_3^{'}=i_{o2}+m_1T_2^{'}, \tag{6}$$

$$\frac{T_2^{'}}{T_3^{'}} = \frac{m_2}{m_1}. \tag{7}$$

By applying Eqs. (4), (6), and (7),

$$T_2^{'} = \sqrt{\frac{A_1^{'}}{K}}, K = \frac{m_1(m_2+m_1)}{2m_2} T_3^{'} = \frac{m_1}{m_2} T_2^{'} \tag{8}$$

From Figure 2a and Figure 2b, T_2 and T_3 can be achieved as

$$T_2 = T_2^{'} - \frac{T_s}{4}, T_3 = T_3^{'} + \frac{T_s}{4} \tag{9}$$

The transient time is

$$T_{tran} = T_1 + T_2 + T_3 = \frac{i_{o2} - i_{L1}^{'}}{m_1}(1 + \sqrt{1 + \frac{m_1}{m_2}}). \tag{10}$$

According to Taylor expansion, Eq. (10) approximately is

$$T_{tran} \approx 2\frac{i_{o2} - i_{L1}^{'}}{m_1}. \tag{11}$$

The main goal of this work is to minimize this time.

2.2. Negative load current step change

In this case, the output is depicted in Figure 2c. According to this figure,

$$i_{o2} = \frac{1}{2}(i_{L1} + i_{L2}) - 4\frac{C}{T_s}(v_{o2} - v_{o1}). \tag{12}$$

The charge section $A_1^{'}$ and discharge portion $A_2^{'}$ can be calculated as

$$T_1^{'} = \frac{i_{L1} - i_{o2}}{m_2}, A_1^{'} = \frac{1}{2} T_1^{'}(i_{L1} - i_{o2}), \tag{13}$$

$$A_2^{'} = \frac{1}{2}(T_2^{'} + T_3^{'})(i_{o2} - i_{L3}), i_{L3} = i_{o2} - m_2 T_3^{'} = i_{o2} - m_1 T_2^{'} \tag{14}$$

Similar to positive load step change $A_1^{'} = A_2^{'}$ and from Eqs. (8), (13), and (14) $T_2^{'}$ can be derived as

$$T_2^{'} = \sqrt{\frac{A_1^{'}}{K}} = \frac{m_2(m_2+m_1)}{2m_1} T_3^{'} = \frac{m_2}{m_1} T_2^{'}, \tag{15}$$

$$T_2 = T_2^{'} + \frac{T_s}{4}, T_3 = T_3^{'} - \frac{T_s}{4}, \tag{16}$$

where the transient time is

$$T_{tran} = T_1 + T_2 + T_3 = \frac{i_{L1} - i_{o2}}{m_2}(1 + \sqrt{1 + \frac{m_2}{m_1}}). \tag{17}$$

Similar to Eq. (10),

$$T_{tran} \approx 2\frac{i_{L1} - i_{o2}}{m_2}. \tag{18}$$

3. Implemented architecture based on predictive control

In recent decades model predictive control (MPC) has been studied extremely, so it has an important background in developing several advantages. Particularly, it can be used in multiple processes and is easy to be applied in multivariable systems. Moreover, it has low limitations in the nonlinear control systems [16].

In switching power converters and electrical drive systems, the time constants are in the range of milliseconds and microseconds. For this reason, much higher sampling rates are necessary for controllers in this field, which also leads to much higher hardware requirements. However, according to Moore's law, the number of components in integrated circuits doubles every two years and with them the available computational power in microcontrollers. This means that MPC, even in the field of switching power converters and electrical drives, will become feasible on standard industrial controllers. Because of this, MPC for electrical drive systems has become more popular in the research community in the last years. The MPC techniques that are applied to switching power converters are assorted into two main classes: continuous control set MPC (CCS-MPC) and FCS-MPC [17–19]. In the first class, the switching states generated by the modulator start from the continuous output of the predictive controller. In the second class, the FCS-MPC approach takes benefit of the confined amount of switching modes in the power converter for finding the optimized state since a discrete form is applied to calculate the response of the system. The switching operation that minimizes a cost function is lastly chosen to be used in the following sampling moment. The main advantage of FCS-MPC is a straight utilization of the control response to the switching converter without needing a modulation circuit [16].

In this paper, the DTFC is controlled using MPC. Although MPC controllers solve an open-loop optimal control problem, the MPC algorithm is repeated in a receding horizon fashion at every sampling time, thus, providing a feedback loop and potential robustness with respect to system uncertainties.

A clear FCS-MPC scheme for voltage control of a DTFC is presented in Figure 1. As displayed in this figure, the load current ($i_L[k]$) and output voltage ($v_o[k]$) are measured and determined by the predictive model. In this section $T[k+1]$ will be predicted. In the minimization section by using a cost function the predicted time and its reference ($T^*[k+1]$) will be matched. The cost function is determined as the error between the predicted time and its reference for each switching state and is shown as $g = |T - T^*|$. Here, T is the predicted time and T^* is its reference. Eventually, the switching state that minimizes the cost function is applied to semiconductor MOSFET switches (S_1, S_2).

In this portion, architecture design and FPGA implementation of the digital controller based on fixed-point computation with minimal functional unit usage are presented. The purpose of the design is to estimate the transient time in fixed-point calculation based architecture for various word lengths. The components of architecture were coded in VHSIC Hardware Description Language (VHDL). As a proof of concept, the proposed architecture is synthesized on a Xilinx Virtex II platform by which all required calculations are performed on-fly and corresponding control signals are produced for the power switches. The FS-MPC flowchart, which is deployed on the hardware, is shown in Figure 3. In this flowchart output voltage (Vo) and inductor current (i_L) are inputs and optimum switching states (S_1, S_2) are outputs. Since there are two switches, there exist four switching states in this flowchart. In the algorithm, the state that produces minimum cost function is selected. The optimum value for cost function (g) is a near-zero value. For achieving this target, at the beginning of the algorithm, the optimal cost function (g_{op}) is equal to ∞. T^* is the reference for transient time, which is 30 μs for all cases, and T is the transient time, which is estimated from Eq. (11) for positive load current step change, and from Eq. (18) for negative load current step change.

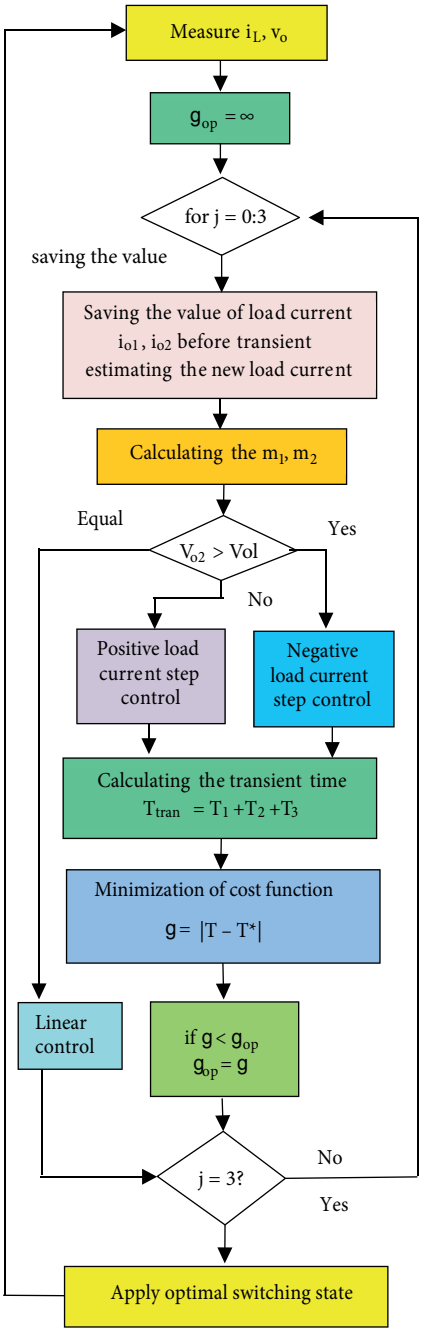

Figure 3. Flowchart of the FS-MPC computations.

The scheduling diagram for computing cost function in negative and positive states is represented in Figure 4. In this scheduling diagram, there are several steps to calculate the output. In this diagram, only two adders (with green and yellow colors), two multipliers (with red and blue colors), and three registers are used. The constant values of a, b, c, d, e, f, g, h, j, and k are obtained from Eqs. (2)–(12).

The hardware implementation of the controller is depicted in Figure 5, which includes a control unit (sequencer), counter, minimization of the cost function, and data path sections. Data path and required

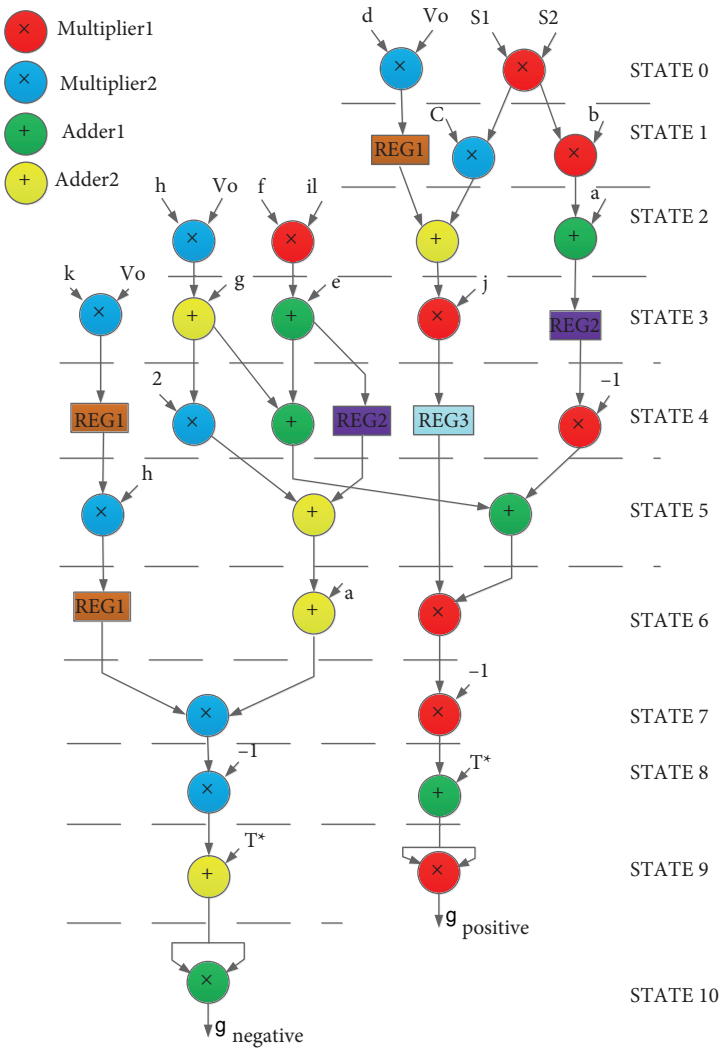

Figure 4. Scheduling diagrams for computing cost function.

functional units are determined based on scheduling and their mapping to the proposed hardware. The sequencer, which is essentially a finite state machine (FSM), produces control signals for the functional units to operate based on the control algorithm. The counter provides four switching states. In this figure, the architecture of computation units is presented, which contains two multipliers (MUL1, MUL2), two adders (ALU1, ALU2), multiplexers (MUXA1, MUXA 2, MUXM1, MUXM 2, MUXR1–3), and three registers (REG1–3). In the minimization section, the state that produces minimum cost function (optimal state) is selected and finally applies to MOSFET switches. Since the hardware works in a discrete space, the cost function (g) in discrete form is

$$g\left[k+1\right] = \left|T^{*}\left[k+1\right] - T\left[k+1\right]\right|, \tag{19}$$

where T^{*} is the reference for T_{tran}, which is 30 μs for all cases, and T is the predicted T_{tran}, which is calculated by the algorithm. The delay generated by the controller, gate drivers, and semiconductor switches is negligible. Table 1 displays used resources in the designed architecture for several word lengths.

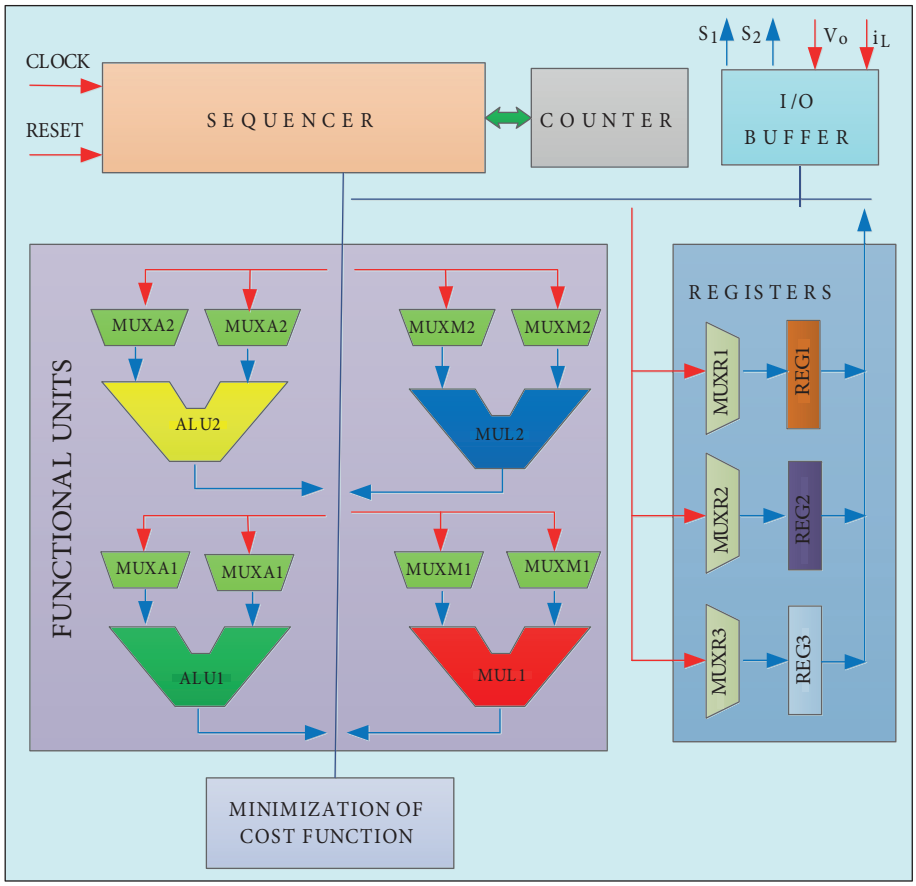

Figure 5. Digital architecture of the DTFC controller.

Table 1. Required hardware resources.

Word length		40-bits	32-bits	22-bits
Area (Slices)	Multiplier	133	112	94
	Adder	118	99	76

4. Results

In this part, calculation precision of the designed digital FCS-MPC controller is concluded. This controller senses the output voltage online. If output voltage has an overshoot (negative load current step), the frequency of gate signals will be decreased until the output voltage returns to its reference, and if output voltage has an undershoot (positive load current step), the frequency of gate signals will be increased until the output voltage returns to its reference. For this goal, several cases are considered for load current conditions and in every case, different word lengths with several integers and fraction parts are checked. In each word length, one bit is rated as a sign bit. The word length and its parts are chosen based on the nature of numbers and their corresponding calculations. For word lengths greater than 40 bits, round-off errors have no effect on the outputs' accuracy, but the system cost will be raised and computation speed will be decreased. For word lengths less than 22 bits, the accuracy of outputs is severely erroneous and would not be acceptable. To find an optimal word length, one should consider a trade-off between the output precision, computation speed, and implementation cost of the

digital controller. Here voltage overshoot–undershoot and transition time (T_{Tran}) are considered as accuracy cost measures. In this converter $V_{in} = 20$ v, $f_s = 250$ kHz, $C = 100$ μ_f, $L = 15$ μ_H, and $V_o = 5$ V.

To evaluate the performance of the controller, negative and positive load current step changes in simulation and experimental states are considered.

4.1. Simulation results

Simulation is performed by MATLAB/Simulink (The MathWorks, Inc., Natick, MA, USA) to confirm the effectiveness of the introduced control algorithm.

4.1.1. Negative load current step

If the negative load current change is smaller than 3 A, approximately for every word length, voltage undershoot–overshoot will be negligible. If negative load current deviation is greater than 3 A we observe overshoot in output voltage. In Figure 6a load current has changed from 5 A to 1 A and to confirm the performance of the proposed method, various word lengths are verified. The efficiency of the converter in this method is 86% and nearly constant for every word length.

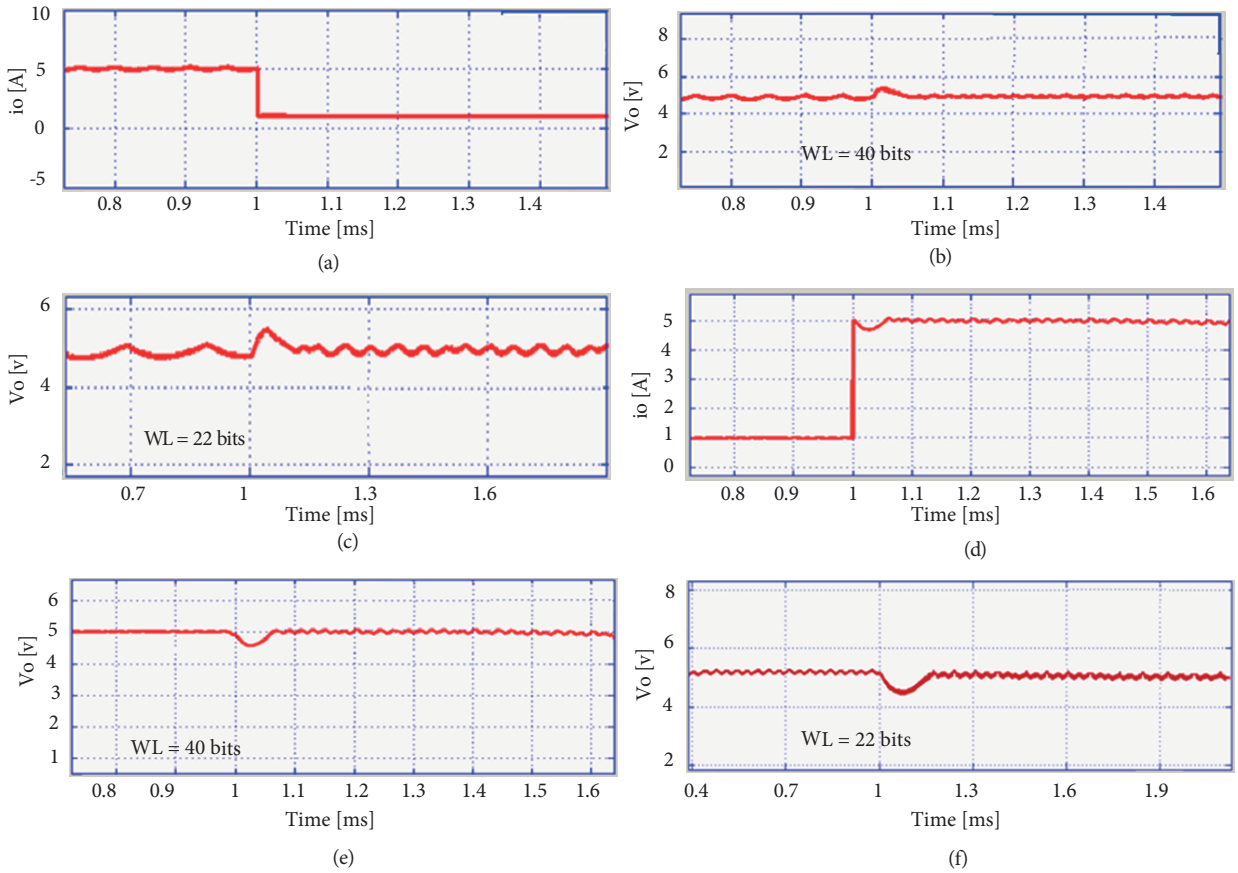

Figure 6. Simulation results. Negative load current step (a, b, c). Positive load current step (d, e, f).

4.1.1.1. Negative load current step and WL = 40 bits

In Figure 6b output voltage for this case is represented. At t = 1 ms load current changes from 5 A to 1 A. It can be observed from this figure that overshoot of the output voltage is 0.2 V and recovery time is 30μs. Here integer length and fraction length are 17 bits and 22 bits, respectively.

4.1.1.2. Negative load current step and WL = 22 bits

In this case, integer length and fraction length are 4 and 17 bits, respectively. Here at t = 1 ms load current has changed. The results are represented in Figure 6c. According to the figure, the accuracy of output voltage has decreased, because the precision of computations has reduced. The overshoot of output is 0.5 V and recovery time is $110\mu s$.

4.1.2. Positive load current step

If positive load current deviation is under 3.5 A, the output voltage approximately has no change. If positive load current changes more than 3.5 A, an undershoot in output voltage will be observed. In Figure 6d, we consider a situation in which output current changes from 1 A to 5 A. In this state, several word lengths are verified.

4.1.2.1. Positive load current step and WL = 40 bits

In Figure 6e results for this case are represented. At t = 1 ms load current changes from 1 A to 5 A. It can be perceived from the figure that undershoot of the output voltage is 0.35 V and recovery time is 60 μs. Here integer length is 17 bits and fraction length is 22 bits.

4.1.2.2. Positive load current step and WL = 22 bits

In this case, the results are shown in Figure 6f. Integer length is 4 bits and fraction length is 17 bits. As can be seen, the accuracy of output voltage has decreased, because the precision of computations has reduced. Undershoot of output is 0.6 V and recovery time is $150\mu s$.

4.2. Experimental results

This section evaluates computation precision of the practical architecture for the control system. Digital circuits are implemented on a Xilinx Virtex-II Pro development board. For the power circuit, we use 7N60 MOSFETs, 1N5408 diodes and AD977A analog to digital converters (ADCs). Figure 7 displays oscilloscope photographs of the output voltage under negative and positive load step changes for various word lengths. Here details of the signals (WL, integer length, and fraction length) are similar to simulation results. Signals are physically produced and observed on the oscilloscope. This controller senses the output voltage online, and if output voltage has an overshoot (negative load current step) or an undershoot (positive load current step), the digital controller setting the frequency of gate signals until the output voltage returns to its reference.

The output results of the implemented digital controller for all situations are displayed in Table 2. According to this table, there is a trade-off between word length and output accuracy. For larger word length, there is smaller overshoot–undershoot and transient time.

Results of CBC and linear methods are compared and displayed in Table 3. It can be perceived from this table that, in each state, the output results of the present study are better than those of other studies; therefore, it shows the precision of the controller design and its performance.

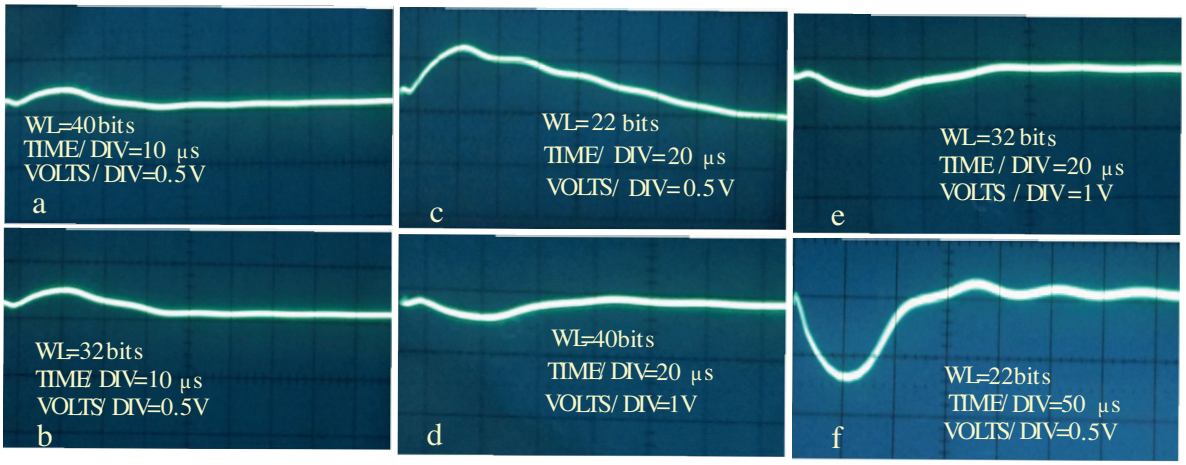

Figure 7. Experimental results. Negative load step changes (a,b,c). Positive load step changes (d,e,f).

Table 2. Fixed-point implementation results for various word-lengths.

Word length	Integer	Fraction	Overshoot in negative load step(V)	Undershoot in positive load step(V)	$\mathbf{T_{tran}}$ in positive load step (μs)	$\mathbf{T_{tran}}$ in negative load step (μs)
40	17	22	0.20	0.35	60	30
32	13	18	0.22	0.40	60	30
22	9	12	0.50	0.60	150	110

Table 3. Comparison between output accuracy of this work and other works.

Word length	40	32	22
Overshoot in this work (V)	0.2	0.22	0.50
Overshoot in CBC method (V)	0.6	0.6	0.6
Overshoot in linear method (V)	2.1	2.1	2.1
Undershoot in this work (V)	0.35	0.4	0.6
Undershoot in CBC method (V)	0.8	0.8	0.8
Undershoot in linear method (V)	1.6	1.6	1.6
Transient time in this work (μs)	30	30	110
Transient time in CBC method (μs)	40	40	40
Transient time in linear method (μs)	180	180	180
Efficiency of this work	86%	86%	86%
ΔIo/Io of this work	80%	80%	80%
ΔIo/Io of CBC and linear methods	50%	50%	50%
ΔVo/Vo of this work	4%	4.4%	10%
ΔVo/Vo of CBC method	5%	5%	5%
ΔVo/Vo of linear method	17.5%	17.5%	17.5%

5. Conclusion

In this article, a new low-cost and flexible architecture of a digital controller has been presented for optimizing dynamic response of a DTFC. The utilized functional units are only two adders and two multipliers. The designed controller uses a linear control algorithm under the steady state situations and the CBC and FCS-MPC algorithms under the transient situations. Hereby using fixed-point computations, the controller has been designed. The hardware is examined with various word lengths and loading conditions to show the controller design precision. The main purpose of the system is to minimize the transient time and overshoot–undershoot of the output voltage. If load current deviations are under 3.5 A, the output voltage approximately has no change, and if load current deviates more than 3.5 A, we will observe overshoot and undershoot in output voltage. Presented results show more accuracy in the controller computation compared with previous works.

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